IN THE CLAIMS

1-34. PLEASE CANCEL

35. (CURRENTLY AMENDED) A split-gate flash memory cell having a trench source with tilted walls comprising:

~~a substrate having a source region;~~

~~a split gate flash memory cell on said substrate;~~

~~a trench source in said source region;~~

~~a gate oxide layer over the inside walls of said trench source; and~~

~~a laterally enlarged diffused area of said source region.~~

a substrate having a top surface;

a gate oxide formed on said top surface of said substrate;

a pair of floating gates formed on said gate oxide;

an interpoly oxide conformally formed over each of said pair of floating gates;

a control gate formed over each of said pair of floating gates;

a trench formed within said top substrate between said pair of floating gates, said trench having tilted walls extending downward within said substrate from said interpoly oxide conformally formed over said pair of floating gates and terminating at the narrow bottom of said trench;

a thermal oxide layer conformally lining said tilted walls and narrow bottom of said trench;

a source region extending from said titled walls and narrow bottom of said trench to a laterally enlarged diffused area under each of said pair of floating gates.

36. (ORIGINAL) The split-gate flash memory cell of claim 35, wherein said trench has a depth between about 200 to 600 A.

37. (CANCELLED)

38. (ORIGINAL) The split-gate flash memory cell of claim 35, wherein said tilted walls have an included angle between about 10 to 45 degrees.

39. (CANCELLED)

40. (CURRENTLY AMENDED) The split-gate flash memory cell of claim 35, wherein said ~~gate~~ thermal oxide layer has a thickness between about 60 to 80 A.

41. (CURRENTLY AMENDED) The split-gate flash memory cell of claim 35, wherein said laterally enlarged diffused area spans at least one-half the width of each of said pair of floating gates. ~~said floating gate.~~